UNIVERSITÀ DI PISA

Corso di Laurea Specialistica in
Ingegneria delle Telecomunicazioni

Esame di Laurea

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ON FUTURE AERONAUTICAL COMMUNICATIONS: IMPLEMENTATION OF A REAL-TIME AEROMACS WAVEFORM FOR SOFTWARE-DEFINED RADIOS (SDR)

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- The Software Defined Radio (SDR) approach
- The “SANDRA” Project and the AeroMACS standard
- Implementation of a real-time AeroMACS modulator
- Implementation of a real-time AeroMACS demodulator
- Available HW/SW resources
- Optimization techniques
- Computational results
- Conclusions and perspectives

The Software Defined Radio: main advantages

- Lower development costs
- Quicker "time to market"
- Easier upgrade to further standard evolutions
- Availability of a fully controllable and completely monitored transmitter or receiver chain intended for signal development, testing or integration on a multi-standard modular radio platform
- Possible application to emergency communication systems

The Software Defined Radio: the "fully-software" approach

- All functional blocks are implemented in software (pure C++) on a **General Purpose Proccessor** hardware architecture
- A fully software approach is currently considered viable only for narrowband systems
- For a given computational target, SDR implementations are **highly power inefficient** when compared to their **hardware counterparts**
- ***Forbidden dream:***
  - enable highly **Efficient Radio Signal Processing** through General Purpose, fully programmable **Computing Architectures**
  - Fully Software Radios for **Wideband/High Bitrate** systems on **reasonable power budgets**

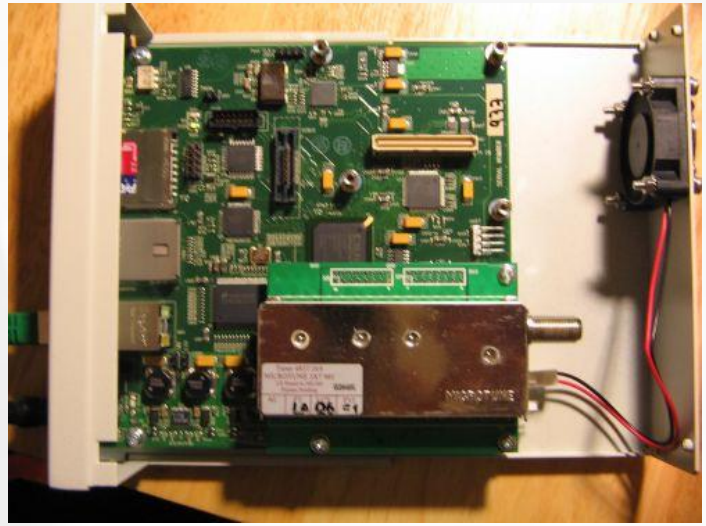
The Software Defined Radio: the USRP2 peripheral

Universal Software Radio Peripheral (USRP)

- HW segment of the GNURadio Project
- General Purpose aquisition/transmission peripheral
- Communication from/towards the host PC via Gigabit Ethernet interface

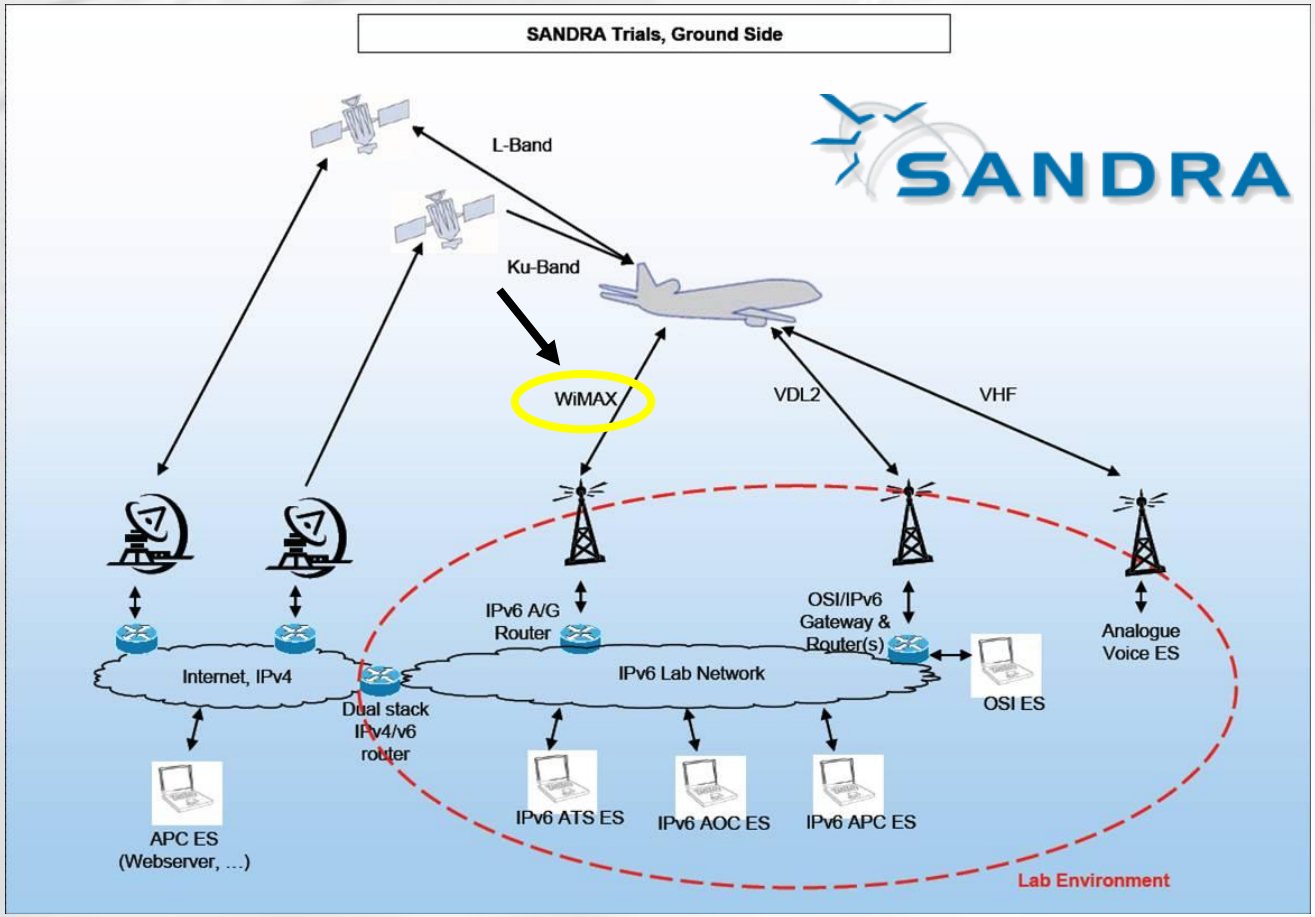
Motherboard:

- 2 Sockets for daughterboards connections
- 2 DACs at 400 Msps (14 bit/sample resolution)
- 2 ADCs at 100 Msps (16 bit/sample resolution)
- 1 Xilinx Spartan FPGA
- 1 Gigabit Ethernet interface
- Max input/output rate: 25 Msamples/s



The "SANDRA" FP7 european project (1/2)

Seamless Aeronautical Networking through integration of Data links, Radios and Antenna



The "SANDRA" FP7 european project (2/2)

- **Target: Integration of aeronautical communication systems using well proven industry standards to enable a cost-efficient global provision of distributed services**
- **Integration at different levels:**
  - **Service integration**
    - Integration of a full range of applications and services (ATS, AOC/AAC, APC)
  - **Network integration**
    - Interworking of different radio access technologies through a common IP-based aeronautical network
    - Interoperability of network technologies (ACARS, ATN/OSI, IPS)
  - **Radio integration**
    - Integration of radio technologies in an Integrated Modular Radio platform
  - **Antenna integration**
    - Hybrid Ku/L band SatCom antenna to develop an asymmetric high data rate DL
  - **WiMAX adaptation for integrated multidomained airport connectivity**

The AeroMACS standard: general features

- Based on IEEE 802.16e-2009 standard
- WirelessMAN-OFDMA PHY
- OFDMA with TDD duplexing mode
- Designed for working also on near-LOS and NLOS scenarios
- Support for advanced power management techniques, interference mitigation/ coexistence, multiple antennas
- For both licensed and license-exempt bands

parameter	options	
Bandwidth	5 MHz	10 MHz
FFT size	512	1024
Sampling frequency	5.6 MHz	11.2 MHz
Carrier frequency	5091-5150 MHz	
Sampling factor	28/25	
Cyclic Prefix	1/8 T_s, 1/16 T_s	
Frame length	5 msec	
Modulations	BPSK, QPSK, 16QAM, 64QAM	

The AeroMACS standard: implemented features

Single User case

- The whole available bandwidth alloccated to a single user

but...

...easily adaptable to a multi-user case

- Partial Usage of the Subcarriers (PUSC) mode

parameter	options
Bandwidth	5 MHz
FFT size	512
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Frame length	5 msec
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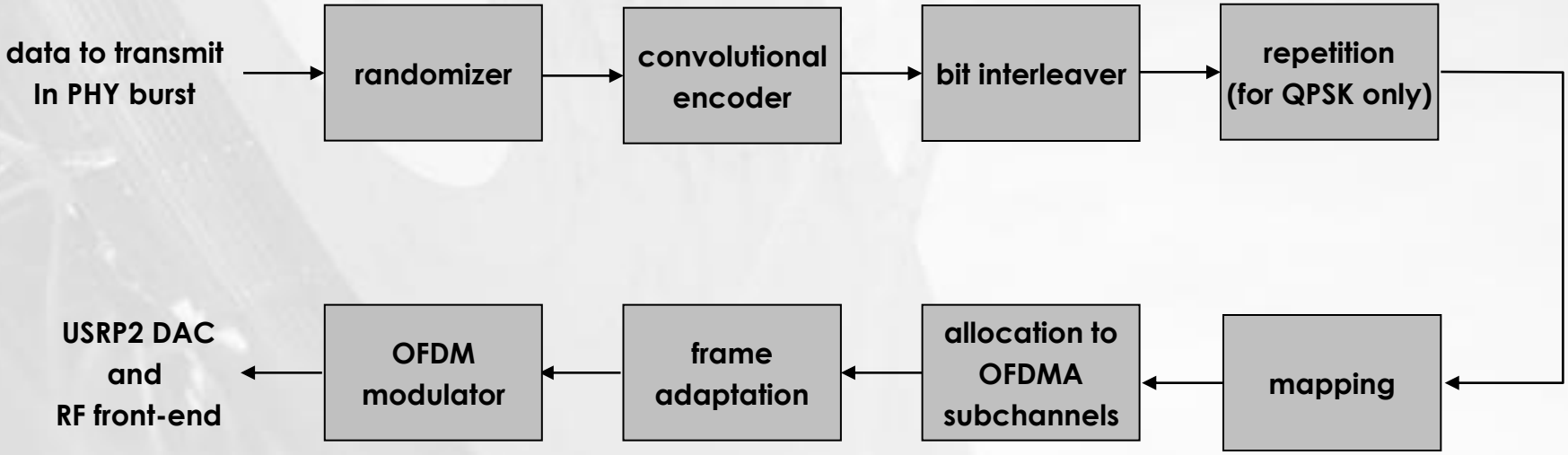
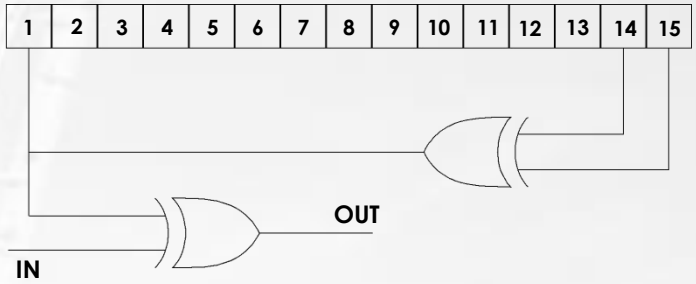
The AeroMACS modulator chain (1/4)

- **Block scheme**

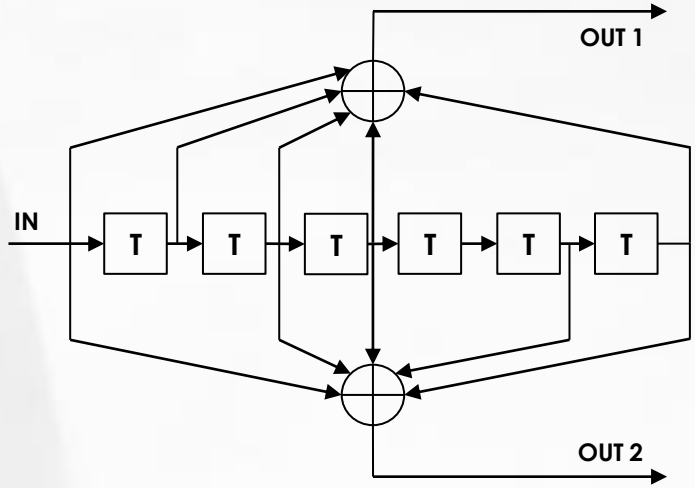


The AeroMACS modulator chain (2/4)

- **Randomizer**
  - Performed on all information data except FCH
  - PRBS generator initialized on each FEC block
  - Preamble not randomized



- **FEC encoder**
  - Tailbiting optimal block convolutional encoding with K=7, r=1/2 and generators $[171, 133]_{oct}$
  - Different FEC block sizes depending on the used modulation (from a minimum of 6 to a maximum of 36 bytes)
  - Larger blocks of coding obtained by concatenation of frequency slots



The AeroMACS modulator chain (3/4)

- **Bit interleaver**
  - Performed on all encoded data bits
  - Interleaving block size = Encoded block size
  - Permutation performed in two steps:
    - adjacent coded bits on non-adjacent subcarriers

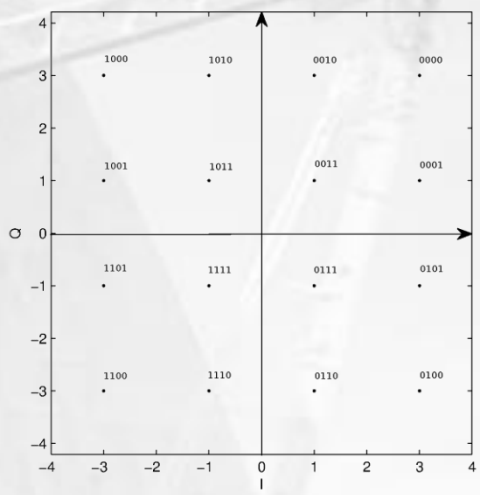
      $m_k=(N_{cbps}/d)\cdot k_{mod(d)}+floor(k/d)$ $\quad k=0, 1, ..., N_{cbps}-1 \quad d=16$
    - adjacent coded bits alternatively onto less or more significant bits of the constellation

      $j_k=s\cdot floor(m_k/s)+(m_k+N_{cbps}-floor(d\cdot m_k/N_{cbps}))_{mod(s)} \quad k=0, 1, ..., N_{cbps}-1 \quad d=16$

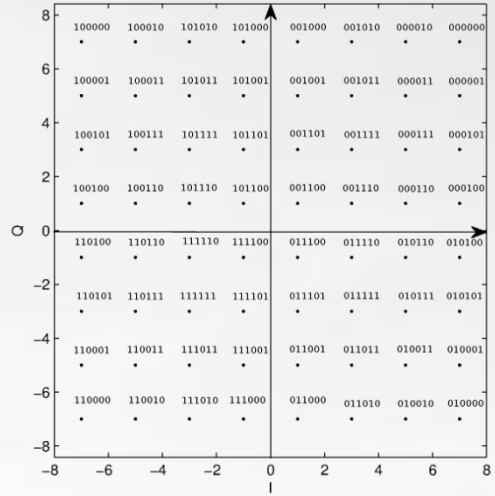
- **Repetition encoder (only for QPSK modulation)**
  - Repetition factor R = 2, 4 or 6
  - The data is segmented into slots, and each group of bits designated to fit in a slot shall be repeated R times to form R contiguous slots following the normal slot ordering that is used for data mapping

An AeroMACS modulator: transmitter chain (4/4)

- **Mapper**
  - BPSK, QPSK, 16QAM and 64QAM Gray encoded constellations

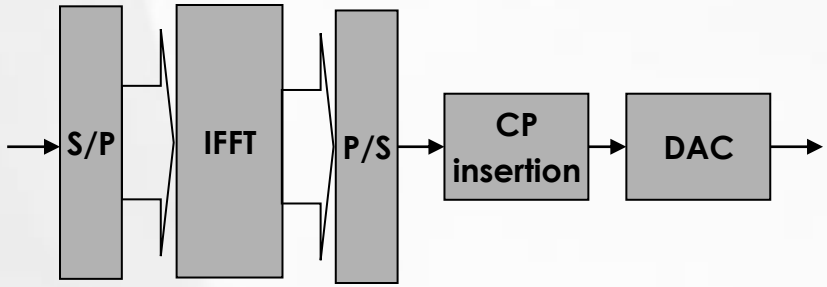


16QAM



64QAM

- **OFDM modulator**
  - 512 subcarriers:
    - 420 active subcarriers
    - 46 left guard subcarriers
    - 45 right guard subcarriers
    - 1 DC subcarrier (null)
  - FFT size: 512
  - 1/8 T_s cyclic prefix (64 samples)

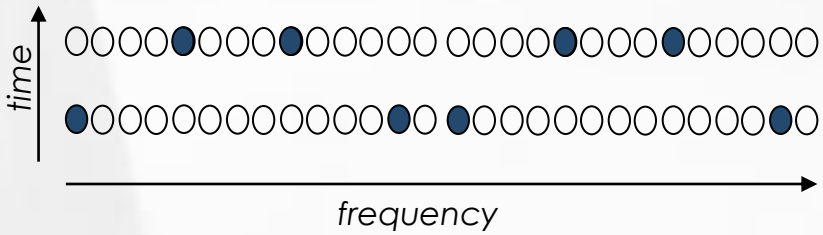


OFDMA Frame Adaptation: subcarriers allocation

- Subcarriers are divided into clusters (14 subcarriers per cluster (2 pilots))
- 2 clusters are grouped into a subchannel
- 1 slot = 1 subchannel over 2 OFDMA symbols
- Subcarriers and subchannels are rearranged into a logical (non consecutive) order

parameter	value
Data subcarriers	360
Pilot subcarriers	60
Number of subcarriers per cluster	14
Number of clusters	30
Renumbering sequence	12, 13, 26, 9, 5, 15, 21, 6, 28, 4, 2, 7, 10, 18, 29, 17, 16, 3, 20, 24, 14, 8, 23, 1, 25, 27, 22, 19, 11, 0
Number of subchannels	15

AeroMACS slot

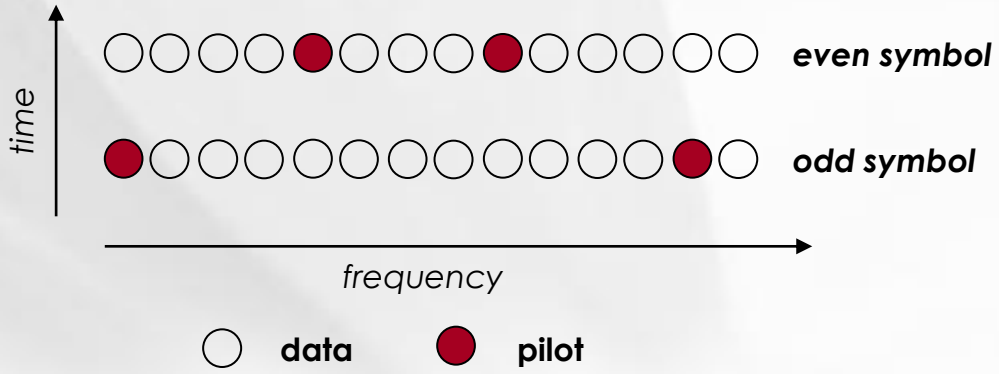


OFDMA Frame Adaptation: reference signals

- A PRBS generator is used to obtain a sequence w_k
- Each subcarrier is multiplied by the factor $2 \cdot \left(\frac{1}{2} - wk\right)$ according to the subcarrier index k
- Pilot subcarriers are BPSK modulated and transmitted with a 2.5 dB boosting:

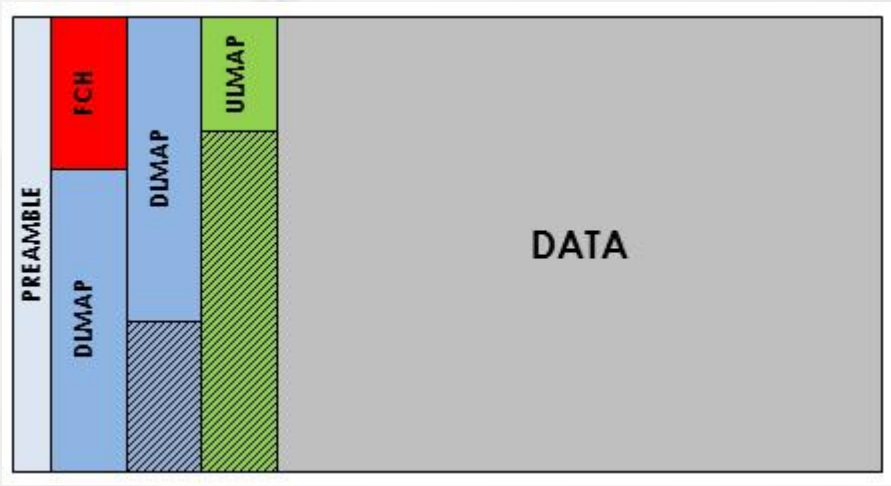
$$Re\{c_k\} = \frac{8}{3} \cdot \left(\frac{1}{2} - wk\right) \qquad Im\{c_k\} = 0$$

- Pilot subcarriers are allocated first within each cluster; the remaining ones are data subcarriers



OFDMA Frame Adaptation: DL subframe structure

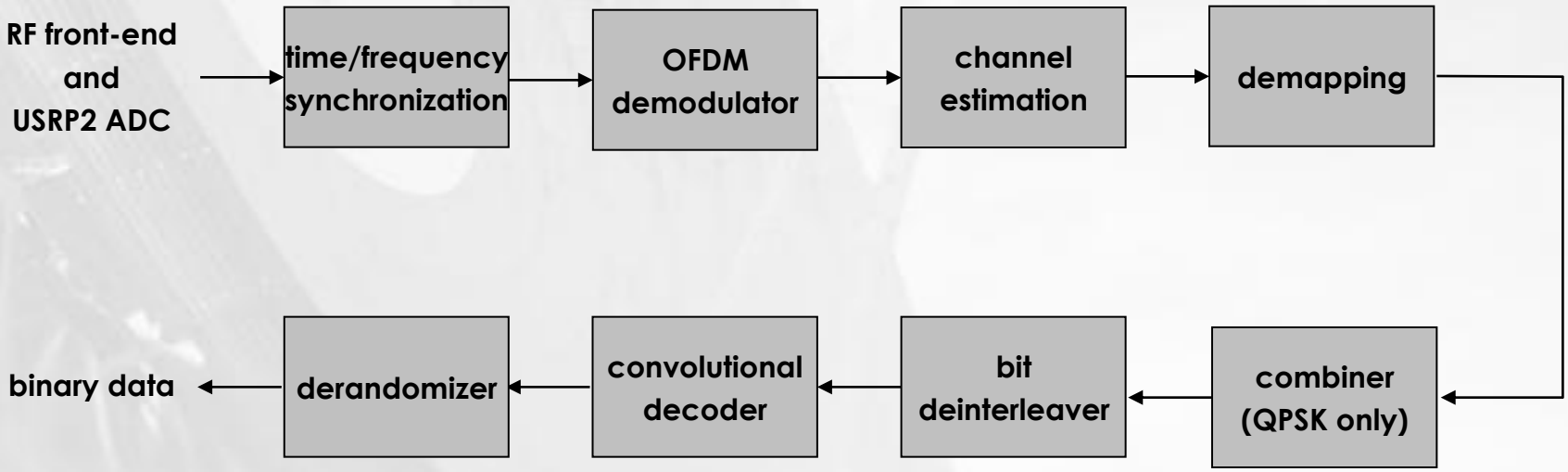
- Simplified structure (Single User)
- All subchannels allocated to a user
- 5 significant fields
  - PREAMBLE – Training Symbol
  - FCH – Frame Control Header
  - DL MAP – Downlink Map Message
  - UL MAP – Uplink Map Message
  - DATA – Data Region (single burst)
- Contents defined by MAC Layer



	length (bytes)	used modulation	coded bits	symbols	repetition	alloc. slots
FCH	6	QPSK, rate 1/2	96	48	4	4
DLMAP	30	QPSK, rate 1/2	480	240	4	20
ULMAP	12	16QAM, rate 1/2	192	48	1	2
DATA	2970	64QAM, rate 1/2	47520	7920	1	165

The AeroMACS demodulator chain

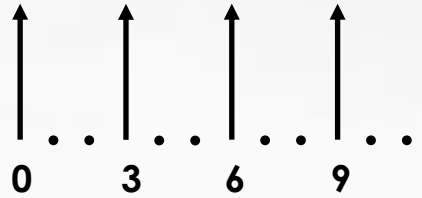
- **Block scheme**



The AeroMACS demodulator: synchronization algorithm (1/3)

Detection of the training symbol

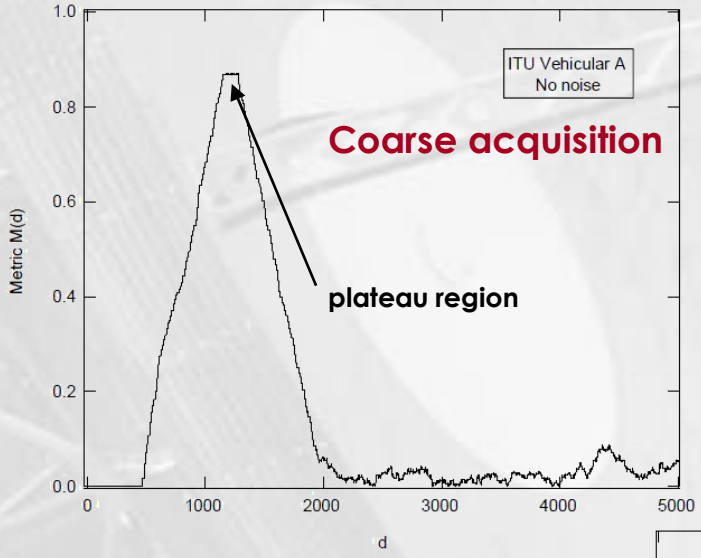
- Coarse timing acquisition
- Preamble modulates only one subcarriers out of three
- Samples in time domain are highly correlated at distance $N_{subcarriers}/3$
- Comparison of a correlation metric M(d) with a suitable threshold λ_0
- λ_0=0.26 gives a false alarm probability of $10^{(-10)}$

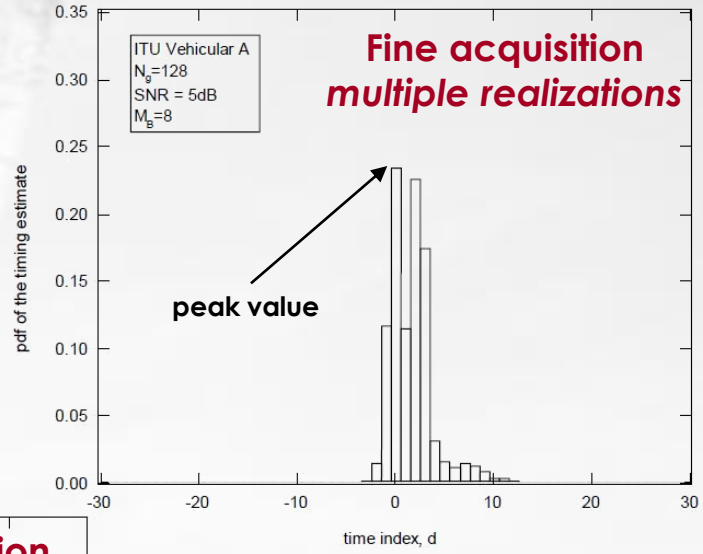


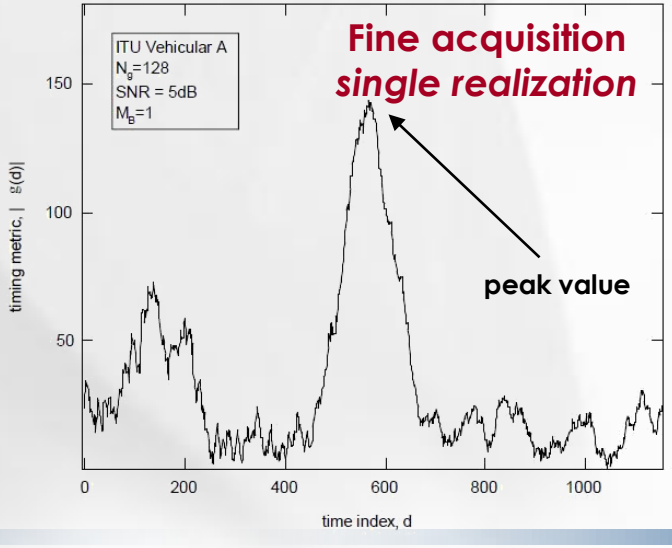
Timing estimation

- Fine timing acquisition
- Cyclic prefix introduced by the OFDM modulator
- Samples in time domain are highly correlated at distance $N_{subcarriers}$
- *argmax*() of the N-lag correlation metric γ(d) averaged onto 10 OFDMA symbols

The AeroMACS demodulator: synchronization algorithm (2/3)







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The AeroMACS demodulator: synchronization algorithm (3/3)

FCFO compensation

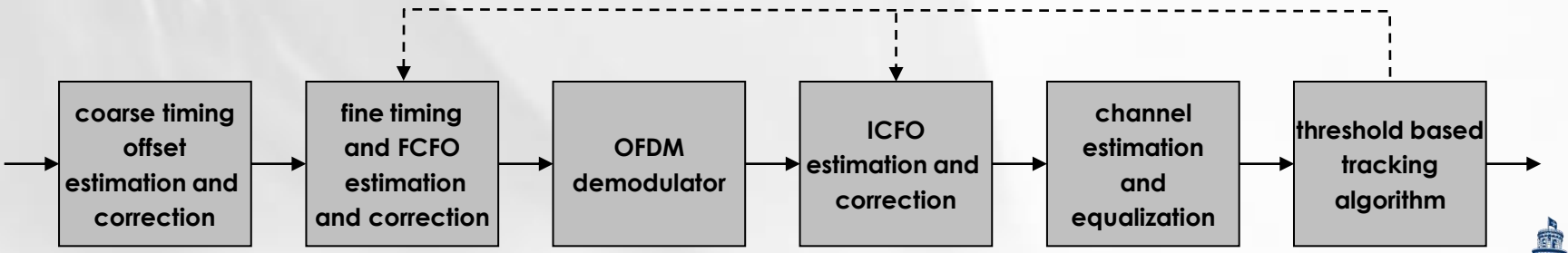
- Discrepancies between local oscillators cause a **Carrier Frequency Offset** (CFO) whose fractional part (FCFO) can be computed as the phase of the **N-lag correlation** $\gamma(d)$
- Compensation is performed in time-domain by a multiplication with an exponential complex oscillation

ICFO compensation and preamble identification

- 114 possible preambles depending on the cell ID and used segments
- Joint detection of the preamble index and integral part of CFO by looking for the *argmax*() of a suitable correlation function

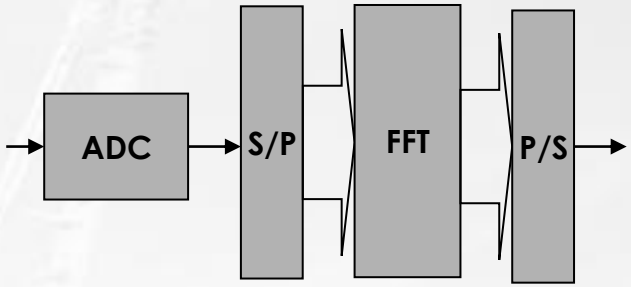
Threshold based Tracking Algorithm

- Computation of a suitable metric exploiting the **non-modulated** DC subcarrier



The AeroMACS demodulator chain: OFDM and decoding (1/2)

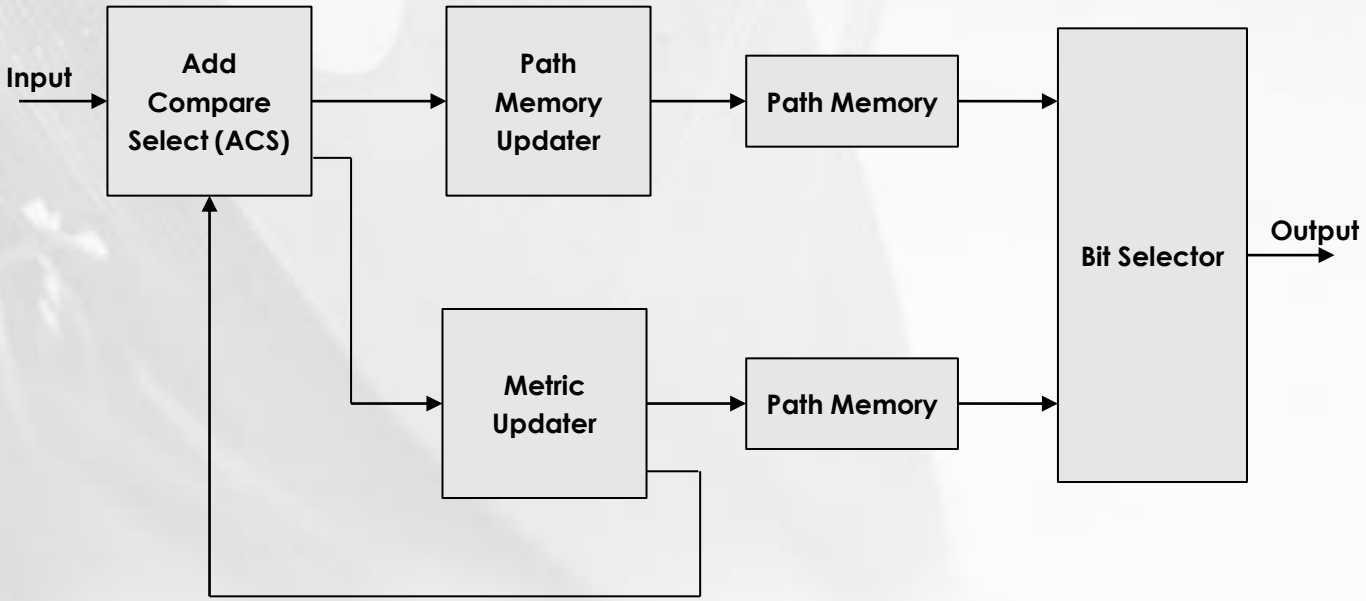
- **OFDM demodulator**
  - Collects 512 received samples
  - Performs DFT through FFT algorithm



- **Demapper**
  - Demapping algorithm based on thresholds and areas of decision
  - Demapping of the mandatory modulations (BPSK, QPSK, 16QAM, 64QAM)
- **Bit deinterleaver**
  - Based on permutations inverse to those defined for the Interleaver
- **De-randomizer**
  - Identical to the Randomizer block

The AeroMACS demodulator chain: OFDM and decoding (2/2)

- **Convolutional decoder: Viterbi algorithm**
- Select the right path on the trellis through an **Add-Compare-Select** algorithm
- Hard decoding: **Hamming distances** used to update accumulated metrics
- Block decoding: FEC blocks of fixed sizes are decoded independently



The AeroMACS demodulator: channel estimation/equalization

- **Channel response expected to be approximately constant over 2 consecutive OFDMA symbols in low-mobility scenarios**

- Estimation of the channel response on the well-known pilot tones:

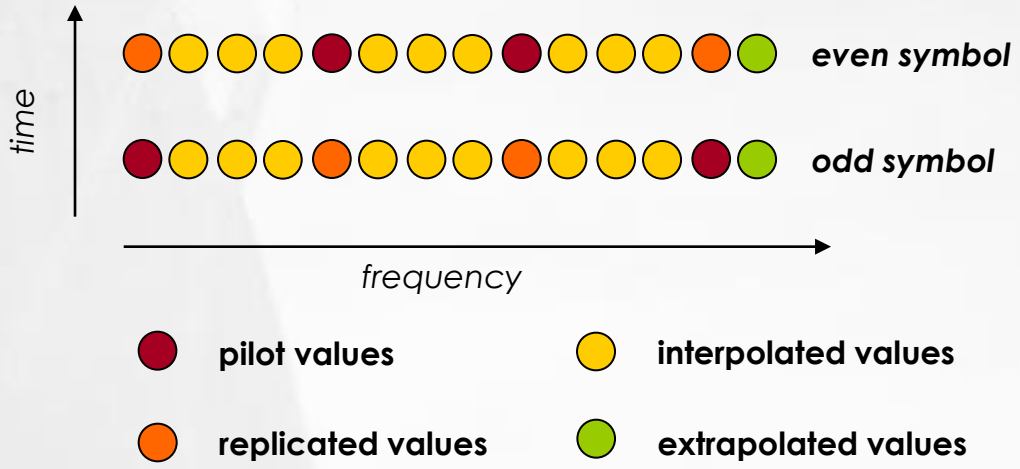
$$\hat{H}_m(p) = \frac{X_m(p)}{c_m(p)}$$

- Linear interpolation in the frequency direction to obtain the other channel gains

$$\hat{H}(n) = \hat{H}(p) + \frac{\hat{H}(p+4) - \hat{H}(p)}{4} \cdot (n-p)$$

- Extrapolation of the channel estimate for n=13 from subcarrier n=12

$$\hat{H}(13) = \hat{H}(12)$$



Available HW/SW resources

- All the signal processing functions of the AeroMACS PHY were developed from scratch as C++ software modules
- Waveform was tested and implemented at:

  DSPCoLa, University of Pisa, Italy

- Hardware resources:
  - *Intel® Core™ 2 Quad Processor Q9400*
  - 4 cores
  - 2.66 GHz clock speed
  - 3 GB RAM
- Software resources:
  - *Fedora 13* 64 bit Operating System
  - gcc version 4.4.5 compiler

Available resources: goal

- **Goal: obtain a real-time fully software implementation of the described functional blocks with the following parameters:**
  - $T_s = (1/\Delta f) \cdot (1 + G)$
  - $\Delta f = f_s / N_{FFT}$
  - $f_s = floor\left(\frac{n \cdot BW}{8000}\right) \cdot 8000$
  - $R_b = \frac{1}{T_b} = \frac{1}{T_{sym}} r \log_2 M = r \log_2 M \frac{(N-NV)}{(N+N_G)} \frac{1}{T_s} = r \log_2 M \frac{(N-NV)}{(N+NG)} \cdot f_s$

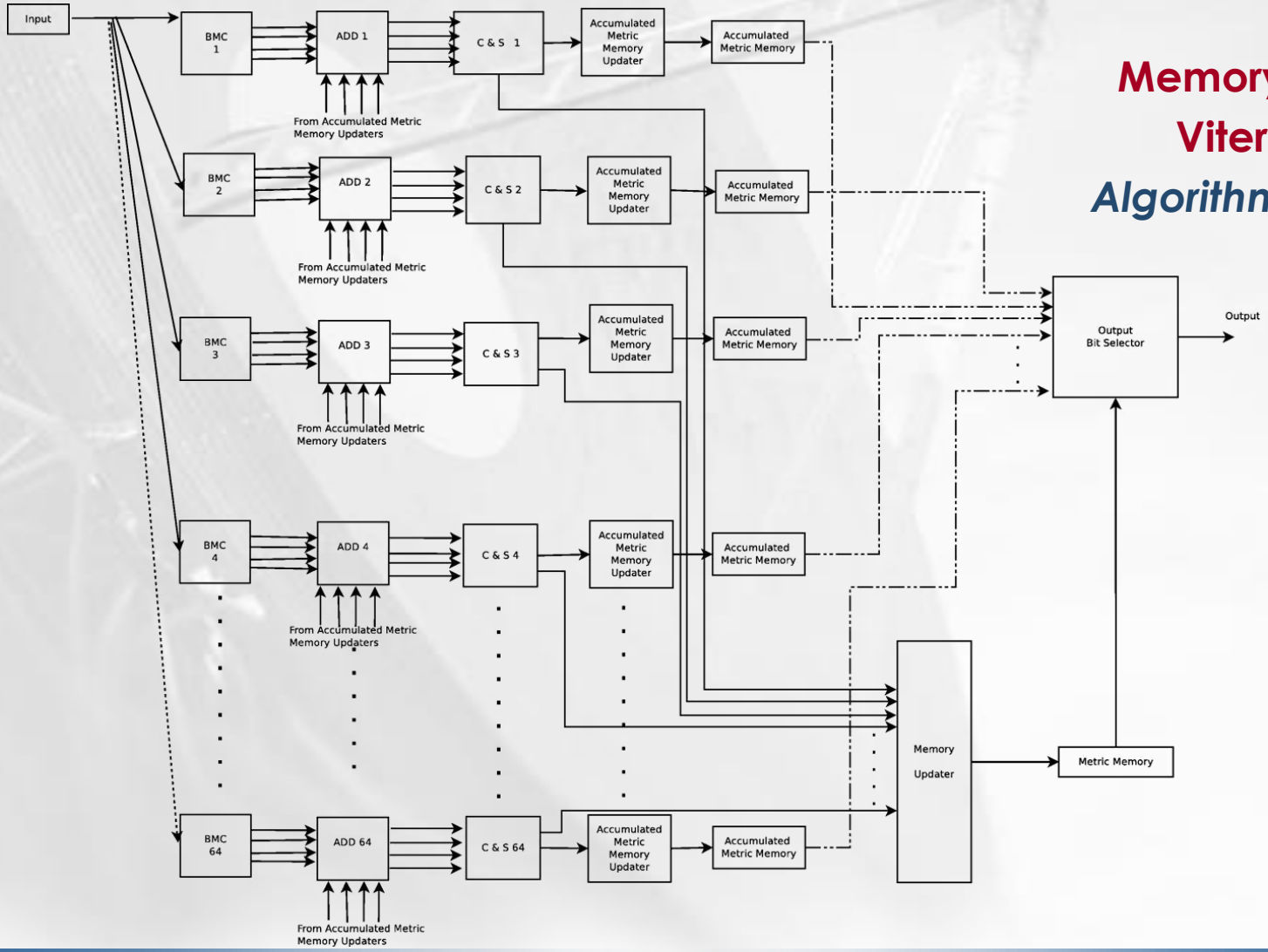
BW	N_{FFT}	N	N_V	N_G	r	M	n	R_b
5 MHz	512	512	92	64	1/2	6	28/25	12,25 Mbit/s

Optimization Techniques: the MA approach

- **Memory Acceleration**

- Optimization technique of the **Space/Time Trade-off** class
- Uses **Memory** as a **Computational Asset**
- Memory is cheap and not power-hungry: increases power efficiency of GPPs
- **Rough idea:** use **Look-Up Tables (LUT)** to store pre-computed results
- Operation Aggregation by Specializing the Memory Space
- **Algorithmic Tools:**
  - ***AS (Algorithm Segmentation)*** – breaks-down a complicated algorithm into smaller, elementary segments
  - ***RTAR (Recursive Table Aggregation Rule)*** – Re-aggregates the algorithms segments into the largest table than can accommodate the algorithm segment(s) into a tabular implementation

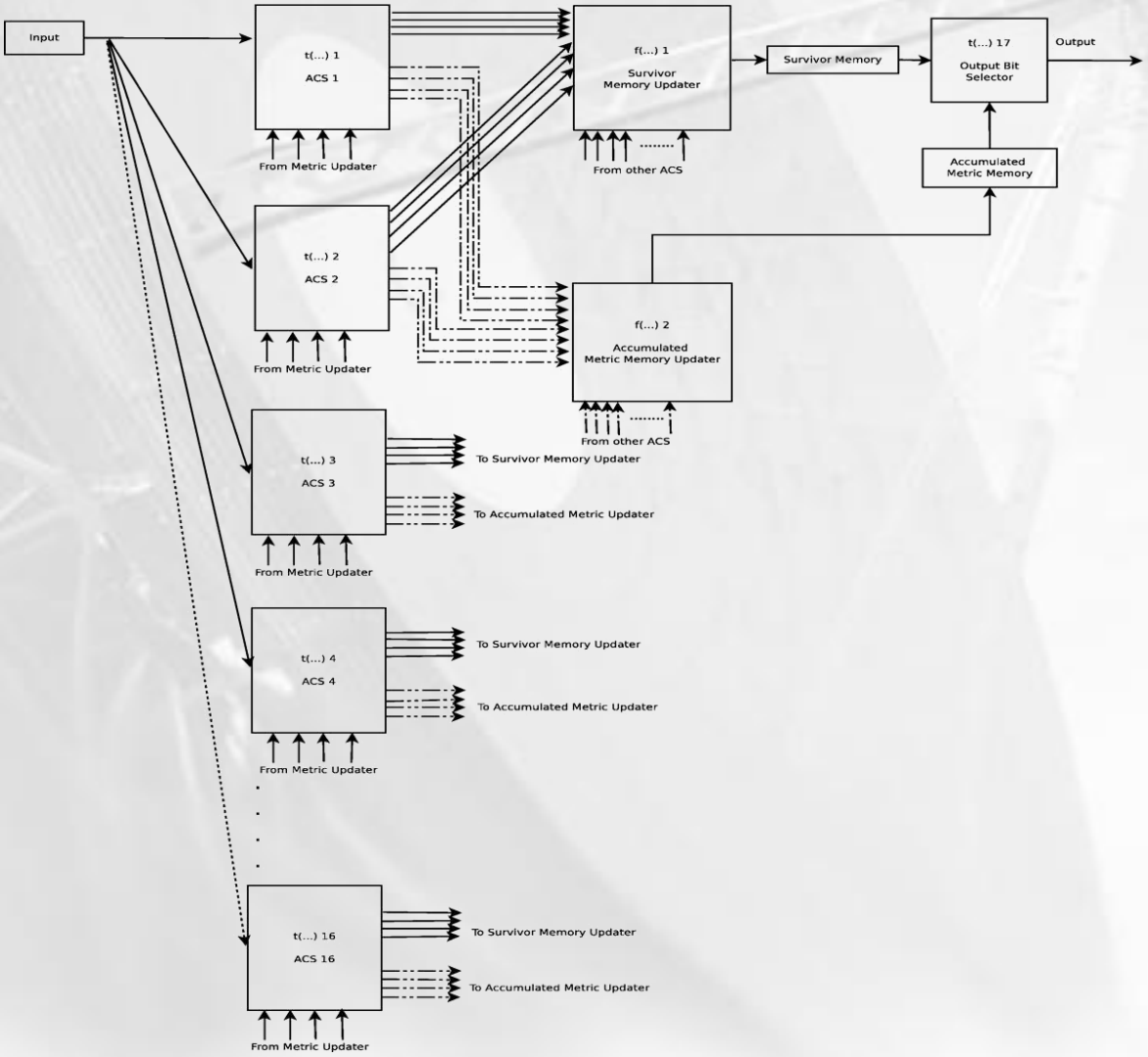
Optimization Techniques: MA Viterbi decoder (1/2)



Memory Accelerated Viterbi Decoder

Algorithm Segmentation

Optimization Techniques: MA Viterbi decoder (2/2)



Memory Accelerated Viterbi Decoder

Recursive Table Aggregation

- *ACS made of 16 contiguous groups of 4 trellis states*
- *Previous states and accumulated metrics of 4 states stored in a single variable*
- *16 metric variables, 64 memory variables*
- *Trellis scanned 2 steps at a time(rate "2/4")*

speed-up factor:

6.8x

Computational Results

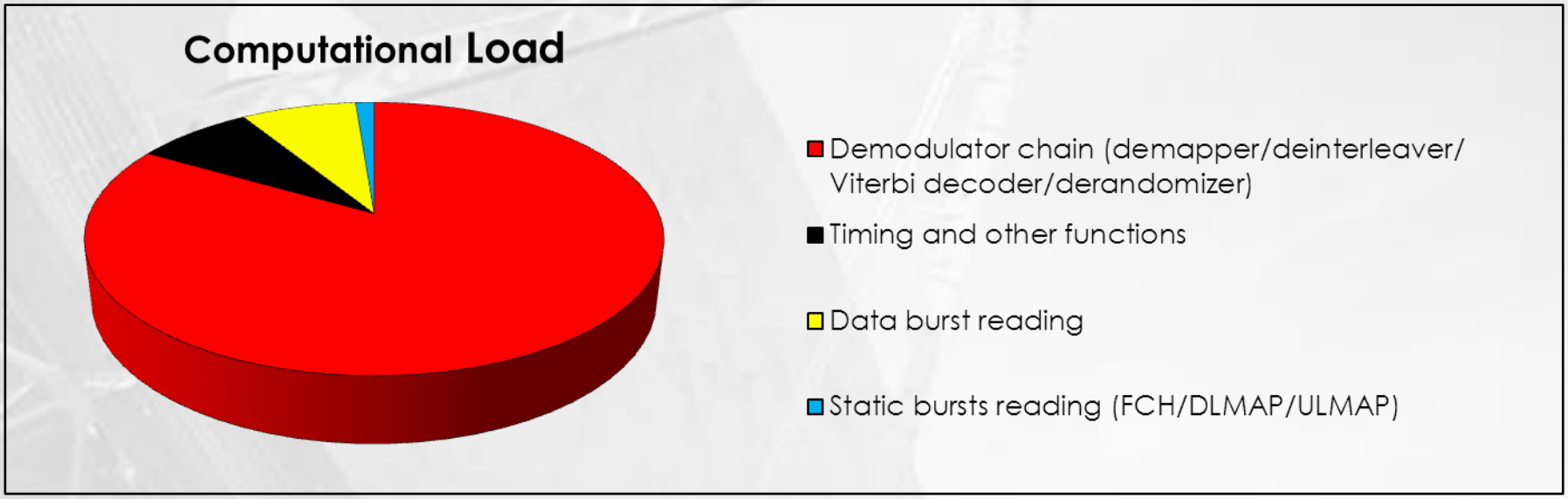
Modulator

- Occupied RAM: **840 kB**
- Computational load: **one 100% busy CPU @ 2.66GHz**
- Target bit rate: **12.25 Mb/s**
- Single-threaded bit rate: **18 Mb/s** ⇨ **Single-thread** software architecture

Demodulator

- Occupied RAM: **129,7 MB**
- Computational load: **one 100% busy CPU @ 2.66 GHz**
- Theoretical bit rate: **12.25 Mb/s**
- Single-thread bit rate: **7.30 Mb/s** ⇨ **Multi-threaded** bit rate: **14 Mb/s**

Computational Results: demodulator



- **Timing and frequency offset correction computational load:**
  - **performed every frame** **4.59 Mb/s**
  - **performed every 5 frames** **6.74 Mb/s**
  - **performed every 10 frames** **7.30 Mb/s**
  - **performed every 20 frames** **7.39 Mb/s**

Conclusions and Perspectives

Conclusions:

- Implementation of a **real-time**, fully-software AeroMACS modulator with a **single-thread** source code
- Implementation of a fully-software AeroMACS demodulator (**0.59 times** the real-time bound) with a single-thread source code
- MA used as the **optimization technique** for reducing computational load

Conclusions and Perspectives

Future works:

- Implementation of a real-time, fully-software AeroMACS demodulator with a **multi-thread** source code
- **RF front-end** setting-up through USRP2 peripheral
- **MAC Layer** software implementation
- Di Dio, Bolognesi, Francone, Luise: *"On Future Aeronautical Communications Standards: a Real-Time, Fully-Software AeroMACS waveform implementation based on the SCA-compliant OSSIE/USRP2 platform"* – Paper accepted for SDR-WInnComm 2013, Washington, January 10, 2013.

SDR - WInnComm
Wireless Innovation Forum Conference on Wireless Communications Technologies and Software Defined Radio

WIRELESS INNOVATION FORUM

DSPCoLa

Thanks for your attention

SANDRA